

Pb phase coarsening in eutectic Pb/Sn flip chip solder joints under electric current stressing

Hua Ye, Cemal Basaran^{*}, Douglas C. Hopkins

*Electronic Packaging Laboratory, Civil Engineering Department, 102 Ketter Hall, North Campus,
SUNY at Buffalo, Buffalo, NY 14260, USA*

Received 22 January 2003; received in revised form 12 November 2003

Abstract

Experimental research on the Pb phase coarsening of eutectic Pb/Sn flip chip solder joint under current stressing is reported. Phase growth is observed under different current densities and temperatures. Higher current density leads to faster grain coarsening. Based on the test results, a grain coarsening equation including the influence of current density is proposed, $d^n - d_0^n = K j^m t$. The current density exponent m is found to be 3, and phase growth exponent n is 5.5. Within our test temperature range, electric current seems to have a greater influence on Pb phase growth of the solder joint than temperature or thermomigration caused by the temperature gradient due to Joule heating during current stressing.

© 2003 Elsevier Ltd. All rights reserved.

Keywords: Phase coarsening; Current stressing; Solder joints; Electromigration

1. Introduction

The reliability of solder joints under current stressing is now gaining more interest than ever as its tendency to carry much higher current density. This tendency is true in both the future high density flip chip packaging and power packaging (Lee et al., 2001; Lee and Tu, 2001; Liu et al., 1999, 2000; Ye et al., 2002a). Electromigration in solder joints has been reported and studied by several researchers recently (Brandenburg and Yeh, 1998; Liu et al., 1999, 2000; Tu and Zeng, 2001; Ye et al., 2002b, 2003a,b,c). The reliability of solder joint under thermomechanical fatigue loading has been extensively studied in recent years (Basaran and Tang, 2001; Basaran and Chandaroy, 1998; Chow and Wei, 1999; Dasgupta and Hu, 1992; Solomon, 1986; Solomon and Tolksdorf, 1996). Morris et al. (1991) stated that the thermal fatigue of Pb/Sn eutectic solder was characterized by microstructural coarsening or phase growth in the fatigue region. Frear et al. (1997) studied the microstructural evolution of the solder and suggested that grain size be a damage parameter to evaluate thermal fatigue lifetime.

^{*} Corresponding author. Tel.: +1-7166452114x2429; fax: +1-7166453733.

E-mail address: cjb@eng.buffalo.edu (C. Basaran).

Pb phase growth was observed in flip chip solder joints under current stressing in our experiments. We expect that this coarsening is also related to the reliability of solder joint under current stressing. Many researchers proposed coarsening models for solder under thermomechanical loading, but the coarsening model for solder under current stressing is still open for discussion due to the lack of experimental results. The understanding of influence of an electric current on metal alloy solid state transformation is still very incomplete. Some examples of influence of an electric current include intermetallic compound formation, precipitation, recrystallization, and grain growth (Conrad, 2000). The phase transformations mentioned here are all diffusion-controlled. Therefore electromigration is obviously expected to be important when considering the influence of an electric current. The atomic flux due to the flow of electric current is given by the Nernst–Einstein equation

$$\vec{J}_{\text{em}} = -\frac{DC}{kT} Z^* e \vec{\nabla} \Psi,$$

where D is pertinent diffusivity, C is concentration, k is boltzman's constant, Z^* is effective valence, e is the electron charge, Ψ is electric potential field. The diffusion flux due to hydrostatic stress gradient in the conductor by Kirchheim (1992) is

$$\vec{J}_{\sigma} = -\frac{DC}{kT} f \Omega \vec{\nabla} \sigma,$$

where f is vacancy relaxation ratio, Ω is atomic volume. The total flux in a metal under current stressing is thus

$$\vec{J}_{\text{tot}} = -D \left(\vec{\nabla} C + \frac{C}{kT} Z^* e \vec{\nabla} \Psi + \frac{C}{kT} f \Omega \vec{\nabla} \sigma \right).$$

Chen, et al. (Chen et al., 1998; Liu et al., 1998) found that, in many diffusion couples, electric current affected the thickness of the intermetallic compound layers which normally formed without a current. They found their experiment results on the diffusion couples were in qualitative accord with electromigration. Xu et al. (1988) reported that a continuous DC current of $\sim 10^3$ A/cm² enhanced the recrystallization rate of cold worked α -Ti and gave a finer recrystallized grain size. At higher annealing temperatures, the current however enhanced grain growth, the degree of coarsening increasing with current density. Maurer and Gleiter (1985) have shown that conduction electrons have an influence on the structure and energy of a grain boundary. Koppelaar and Simcoe (1963) reported that a d.c. current of $\sim 10^3$ A/cm² enhanced the precipitation rate of an Al–4wt.%Cu alloy determined by resistivity measurements. The precipitation rate increases in an approximately linear fashion with current density beyond a critical value of $\sim 10^3$ A/cm². Electric current is also found by researchers (Lai et al., 1989; Lai et al., 1995; Teng et al., 1996) to accelerate crystallization of rapidly quenched amorphous alloys (Fe–Si–B). But until today our understanding of the detailed atomic mechanisms pertaining to the effects of a current on phase transformation is still very rudimentary (Conrad, 2000).

This paper reports the Pb phase growth in flip chip solder joints with different initial phase size, different current density and different stressing temperature. The results are compared to the existing phase coarsening models.

2. Experimental

The test flip chip modules were produced in an industrial lab to attain consistent interconnects representative of volume manufacturing. The test module has a dummy silicon die with only Al conduct trace on it. The silicon die is attached on a FR4 printed circuit board (PCB) through eutectic Pb37/Sn63 solder

joints. The under bump metallization (UBM) is electroless Ni. The copper plates on the PCB provide the wetting surface and electric connection to the solder joints. The solder joints are encapsulated in the underfill between the silicon die and PCB. The thickness of the Al trace is about 1 μm and the width is about 150 μm . The diameter of the solder joint is around 150 μm and the height is about 100 μm . The test module was cross-sectioned and finely polished to the center of the solder joints before current stressing. The ASTM standard E3 (1999b) was applied to the surface preparation. On each module, two solder joints were tested. The solder joints on each test module are named in such a way that current always flows from copper trace through solder joint A into the Al trace on silicon die and then flow through solder joint B out to another copper trace. Fig. 1 shows a schematic of the cross-section of the test module and the direction of current flow in the experiments. Ye et al. (2003b) have shown in their experiment that there is a possibility that a high temperature gradient is maintained in the solder joint during current stressing due to joule heating. This thermal gradient will cause thermomigration always in the direction from hot side (Silicon die side) to cool side (FR4 side). Thus, in solder A, thermomigration is in the same direction of electromigration; and in Solder B, thermomigration is in the opposite direction of electromigration.

During the course of current stressing, the test modules were taken off circuit for scanning electron microscopy (SEM) analysis. Since it is very difficult to measure the temperature on a 100 μm solder joint directly, the temperature of the silicon die was occasionally measured during current stressing with a fine-tipped thermocouple. A coupled thermal–electrical finite element simulation predicted the temperature in the solder joint would be very close (within 10 $^{\circ}\text{C}$) to the temperature on the silicon die in this test module (Ye et al., 2003b). The Pb phase size of solder joints was measured during the course of current stressing following ASTM standard E1382 (1999a). According to ASTM standard E1382, several methods can be used to determine average grain size: grain intercept lengths, intercept counts, intersection counts, grain boundary length, and grain areas. Individual grain area method for two-phase structure is used in this experiment since digital imaging processing software is employed. The area of each Pb phase interior, A_i , on the solder surface is measured for every Pb phase region. The average phase region area, \bar{A}_{Pb} , is determined by:

$$\bar{A}_{\text{Pb}} = \frac{\sum_{i=1}^N A_i}{N_{\text{Pb}}},$$

where N_{Pb} is the total number of Pb phase regions on the solder surface. The average Pb phase region area was measured for each solder joint before and after certain hours of current stressing at room temperature. The average phase area was measured directly on the SEM backscattered images of cross-sectioned solder joint. The area fractions of Pb phase region for initial as-reflowed solder joints, $N_{\text{Pb}}\bar{A}_{\text{Pb}}/A_{\text{Total}}$, are between 26.5% and 29.1% and are in accordance with predicted volume fraction of Pb Phase from phase-diagram (Jung and Conrad, 2001a). Media Cybernetics's image analysis software (2000) *Image Pro Plus*[®] was used to automatically identify the phase region boundary, and measure phase area and average diameter. On SEM backscatter image, the light region is corresponding to the Pb rich region, and dark region is corresponding to the Sn rich region because of their difference in elemental numbers. By setting the gray scale

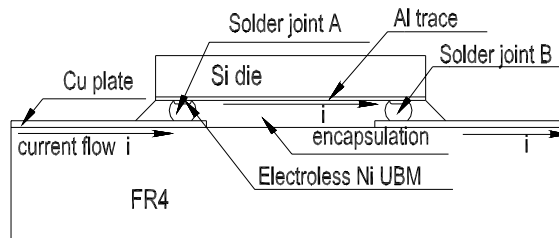


Fig. 1. Schematic cross-section of the test module.

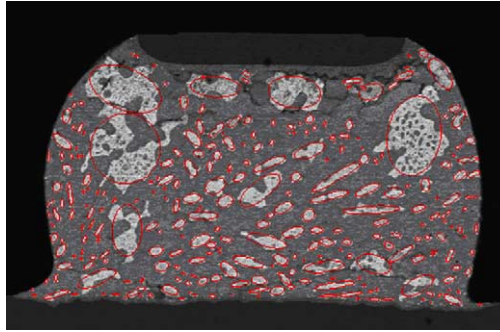


Fig. 2. Pb phase outlined by ImagePro plus.

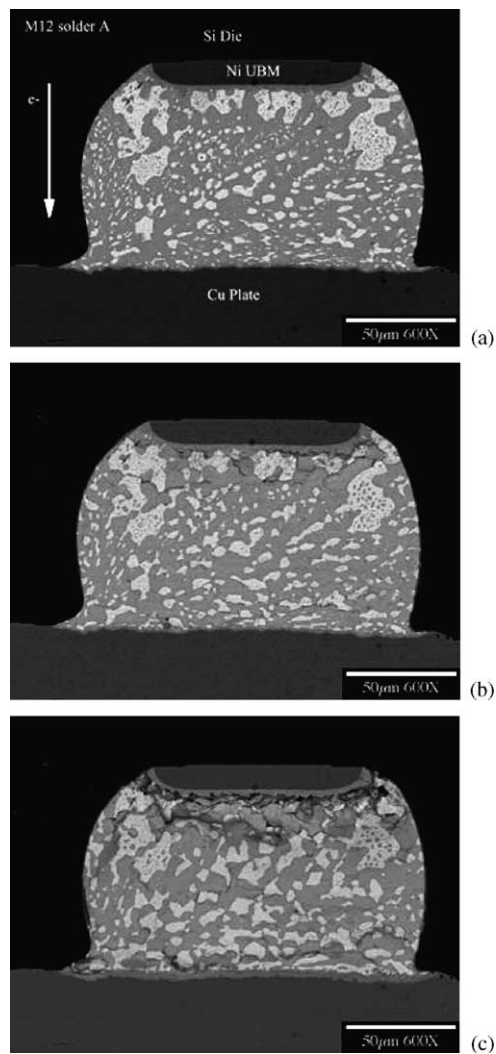


Fig. 3. SEM backscattered image of solder joint A from module #12: (a) initial, (b) 16 h, (c) 36 h.

limits in *Image Pro Plus*®, the Pb rich region boundary can be detected, and average area data measured. The Pb phase region is outlined by the software as shown in Fig. 2.

During the course of current stressing, the average Pb phase size was observed to grow. Voids were observed to nucleate near the cathode side and hillocks observed near anode side. Fig. 3 shows the SEM backscattered image of solder A from module #12 during current stressing, where phase coarsening is clearly shown. Intermetallic compound growth is also clear on the solder/Cu plate interface.

3. Calculation of cross-section area of sectioned solder joint and current density

Before the current stressing, each module is cross-sectioned with a precision diamond saw and then polished to expose the section of the solder joints. It is very difficult to polish to the exact center of the solder joint (as shown in the right part of Fig. 4) even though one checks the polishing progress constantly under an optical microscope. It is more likely for one to polish to somewhere near the center of the solder joint (as shown in the left part of Fig. 4), but not the exact center. Thus the cross-section area (the shaded area in the Fig. 4) of solder joint subject to current stressing varies from joint to joint.

For the purpose of calculating the cross-section area of solder joint, the diameter of each solder joint is assumed to be 150 μm , and the diameter of Ni UBM on Si die side is assumed to be 100 μm . This may not be the case since they may vary from one solder joint to another due to manufacture imperfection. Based on this assumption, we can calculate the cross-section area (the shaded area in Fig. 4) of each polished solder joint by measuring its width and the length of UBM on the polished surface. We use this calculated cross-section area to compute the nominal current density for each solder joint in this paper.

4. Test results

The Pb phase growth of 14 Pb/Sn eutectic flip chip solder joints under different current density from 0.4×10^4 to 1.13×10^4 A/cm² is reported in this paper. In order to compare the phase size growth between different solder joints, normalized phase size will be used. Since we measure the average area of the Pb phase, phase size is defined as the square root of average phase area, $d = \sqrt{A_{\text{Pb}}}$. Normalized phase size is

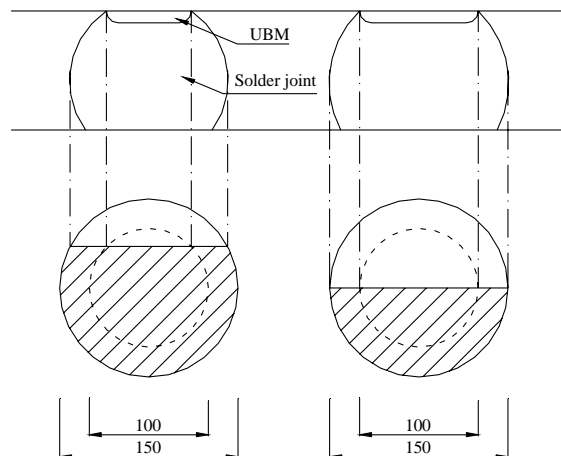


Fig. 4. Schematic view of sectioned solder joint.

further defined as phase size divided by the initial phase size for each solder joint, or d/d_0 , where d_0 is the initial phase size. The initial Pb phase size is measured from the as-reflowed microstructure of solder joint before stressing at room temperature. Thus, every solder joint has a normalized initial phase size of 1. Both the initial Pb phase size and the Pb phase size after certain hours of current stressing were measured at room temperature, since the test module was taken off the stressing circuit for SEM analysis. Because the actual Pb rich phase is a three dimensional microstructure, the measured two dimensional phase size on the polished surface is dependent on the position of polishing. A re-polishing will thus undoubtedly alter the measured phase size even without any current stressing. The phase size reported in this paper does not include any data measured after a re-polishing. If a module is re-polished at a very early stage of current stressing, the initial phase size is taken as the measured phase size right after that re-polishing; but no data is collected after further re-polishing. The solder joints reported in this paper are named as M##A or M##B, where M## indicates the module number as in our original experiments. Letter A or B indicates if it is solder joint A or solder joint B as defined earlier. M8A thus represent solder joint A on module #8. Fig. 5 shows the normalized phase size d/d_0 versus current stressing for all the 14 solder joints. All solder joints except M15A and M15B, which have the lowest current density (0.4×10^4 A/cm²) and temperature (40 °C) in the group, observed Pb phase growth. The current density, temperature, and initial phase size of each solder joint are listed in Table 2 in the following section. The curves in Fig. 5 look scattered because of the different current density in each solder joint.

Fig. 6 shows the normalized phase size vs. stressing time for solder joints with current density between 0.57×10^4 and 0.68×10^4 A/cm² only. The number in the parenthesis in the legend area shows the stressing temperature for each module. It shows that M26A and M26B, with a slightly higher stressing temperature of 105 °C, have a slightly more rapid growth rate than the rest of the solder joints, but it is well within the experimental error range. Fig. 7 shows the normalized phase size vs. stressing time for solders with different current density from 0.4×10^4 to 1.13×10^4 A/cm². The stressing temperatures of these solder joints were between 90 and 100 °C, except M12A (no temperature measured) and M15B (40 °C). It shows very clearly that higher current density leads to more rapid phase coarsening. It is our understanding that, within the temperature range where we tested the specimens, current density seems to be a more prominent factor to

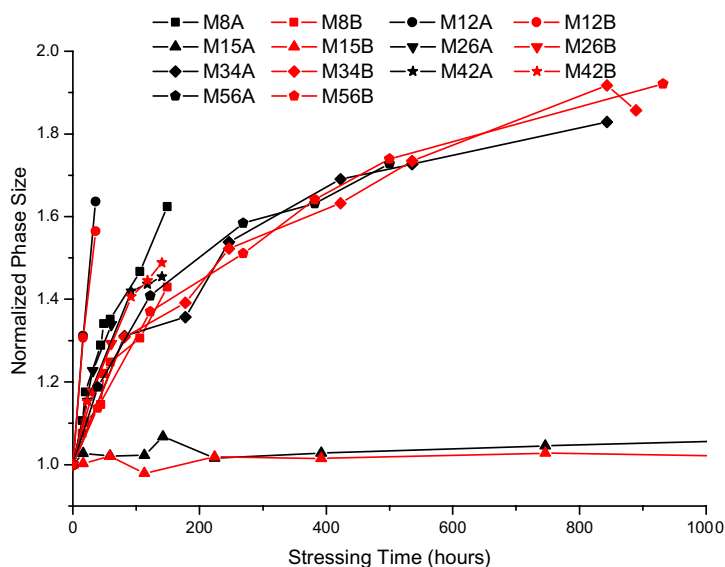


Fig. 5. Normalized phase size vs. stressing time.

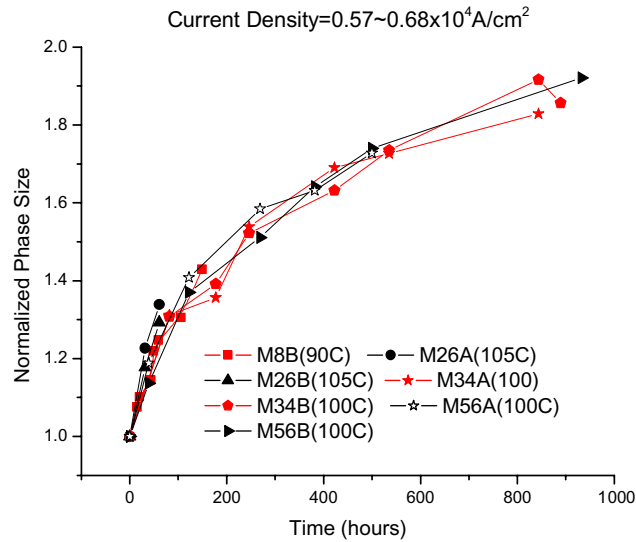


Fig. 6. Normalized phase size vs. stressing time of solder joints with current density between 0.57×10^4 and 0.68×10^4 A/cm².

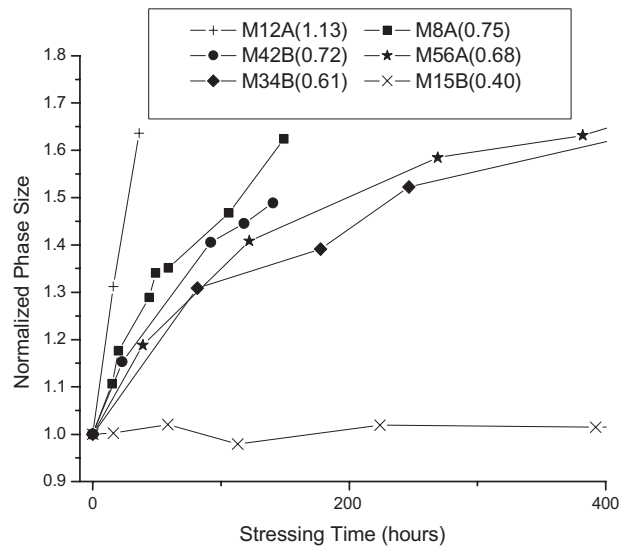


Fig. 7. Normalized phase size vs. stressing time of solder joints with current density between 0.4×10^4 and 1.13×10^4 A/cm².

the Pb phase coarsening than temperature, although temperature certainly has effect on this process because of the Arrhenius relationship between diffusivity and temperature.

5. Discussions

For over a century, researchers have observed, analyzed, and tried hard to model microstructural evolution of polycrystalline material. Understanding microstructure is critical because it governs the

mechanical, thermal, and electrical properties of engineered materials. Burke and Turnbull (1952) proposed the conventional grain growth law for polycrystalline materials as

$$\dot{d} = \frac{K}{d^{n-1}},$$

where d is grain size, \dot{d} is the grain size growth rate, K is the grain boundary mobility parameters, n is a exponential constant, empirically between 1.5 and 9 (Chen and Spaepen, 1991; Ng and Ngan, 2002). Burke and Turnbull further proposed that the parameter K has an Arrhenius form, $K = K_0 e^{-Q/kT}$; where K_0 is a constant, Q is the grain growth activation energy, k is the Boltzman's constant, T is absolute temperature. Integrating Burke and Turnbull's grain growth equation gives

$$d^n - d_0^n = Kt,$$

where d_0 is the initial grain size at the test temperature. Researcher since then elaborated on this grain growth law for different applications. For example, Hacke et al. (1993) proposed a cubic Pb phase coarsening model for eutectic Pb/Sn solder alloy under thermal mechanical fatigue loading,

$$d^3 - d_0^3 = \frac{ct}{T} e^{-Q/kT},$$

where c is a kinetic factor that depends on matrix composition, Q is the activation energy for volume diffusion. Subsequent work by Jung and Conrad (2001b) gave $n = 4.1 \pm 0.15$ and $Q = 39.8$ kJ/mole, which is for grain boundary diffusion. Upadhyayula (1999) modified this model to include the mechanical stress influence as

$$d^3 - d_0^3 = \frac{ct}{T} e^{-q/kT} \left(1 + \left(\frac{\Delta\tau}{c_2} \right)^{n_c} \right),$$

where $\Delta\tau$ is the stress range, n_c is the stress exponent, c_2 is the reference stress.

Unfortunately, these coarsening models cannot be directly used in modeling phase growth of eutectic solder under current stressing since none of them included the influence of electric current. From experiment results as shown in Figs. 5–7, the phase growth of the individual solder joint seems to obey the Burke and Turnbull's exponential growth law. This is verified by re-plotting phase size vs. time on a log–log scale as shown in Fig. 8. It clearly shows that phase size vs. time curves now become close to straight lines in log scale, indicating the powered relationship between phase size and time.

Nonlinear regression procedure is used to determine the exponential n in Burke and Turnbull's coarsening law for each solder joint from the experiment results. The Burke and Turnbull's grain growth equation is rewritten as

$$\left(\frac{d}{d_0} \right)^n = 1 + \frac{Kt}{d_0^n},$$

thus

$$\frac{d}{d_0} = \left(1 + \frac{Kt}{d_0^n} \right)^{\frac{1}{n}},$$

where d/d_0 is the normalized phase size used in the experiment. Let $Y = d/d_0$, $X = t$, $B_1 = K/d_0^n$, and $B_2 = n$. We are now using the experimental data of each solder joint to fit equation $Y = (1 + B_1 X)^{1/B_2}$. Table 1 gives the regression results for solder joint M56B. The value of exponent n for solder joint M56B is about 5. The 90% confidence range is from 4.42 to 5.64. Fig. 9 shows the comparison between the test data and fitted curve.

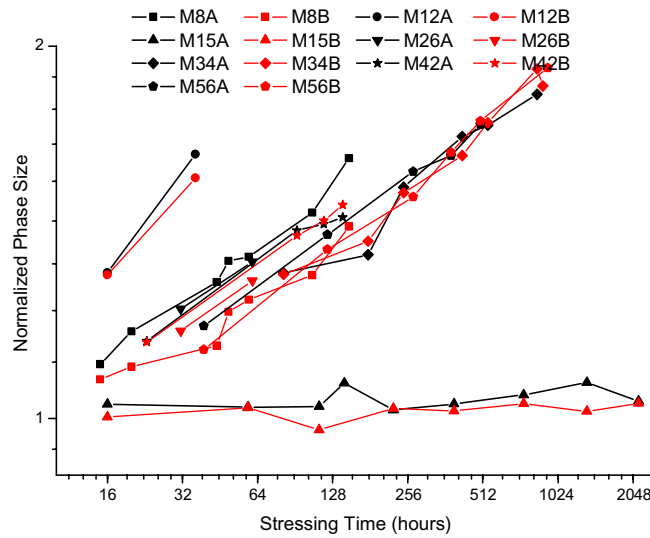


Fig. 8. Log-log plot of normalized phase size vs. stressing time.

Table 1

Regression result for solder joint M56B

Variable	Value	Standard error	<i>t</i> -ratio	Prob(<i>t</i>)	90.00% Confidence limits	
B_1	0.02848	0.00489	5.81611	0.00212	0.01862	0.03835
B_2	5.03381	0.30218	16.65840	0.00001	4.42492	5.64270

The same nonlinear regression procedure was applied on each solder joint and the results are summarized in Table 2 along with the information of current density, temperature, initial phase size for each solder joint. We should mention that for solder joints M12A, M12B, M26A, and M26B, there are only three data points available for each solder joint in the nonlinear regression procedure, which is insufficient for this highly nonlinear regression. For the rest of the solder joints, the phase growth exponent ranges from 4.4 to

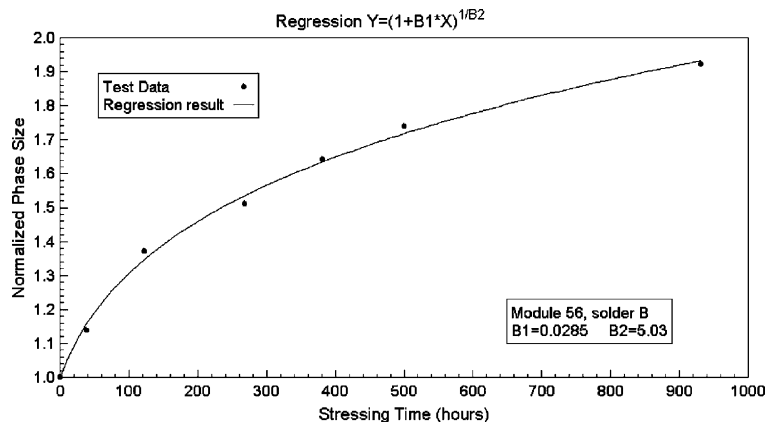


Fig. 9. Nonlinear regression for solder joint M56B.

Table 2

Regression results for $Y = (1 + B_1X)^{1/B_2}$

Module #	Current density (10^4 A/cm ²)	Temperature (°C)	Initial phase size (μm)	$B_1 = K/d_0^n$	$B_2 = n$
M8A	0.75	90	1.88	0.0473	4.41
M8B	0.57	90	1.97	0.0253	4.50
M12A	1.13	n/a	2.66	0.0385	1.77
M12B	0.88	n/a	2.40	0.0704	2.82
M15A	0.40	40	2.8	n/a	n/a
M15B	0.40	40	3.14	n/a	n/a
M26A	0.57	105	2.16	0.0694	5.67
M26B	0.57	105	1.81	0.0282	3.90
M34A	0.62	100	2.32	0.0392	5.73
M34B	0.61	100	2.12	0.0323	5.33
M42A	0.72	120	2.71	0.0719	6.20
M42B	0.73	120	2.52	0.0501	5.20
M56A	0.68	100	1.88	0.0549	6.14
M56B	0.64	100	2.06	0.0285	5.03

6.2. These values are much higher than 3 as proposed in Hacke et al.'s (1993) eutectic solder coarsening model and a value of 4 of later work by Jung and Conrad (2001b). In the earlier section, we mentioned that the possible thermomigration may have the same or opposite direction with electromigration in solder joint A or solder joint B, respectively. But as shown in Table 2, there is no big difference in phase growth exponent n between solder A and solder B for each test module. If the current density in both solder joints in a single module is close to each other, their phase size vs. time curves also looks close to each other. These observations suggest that in our experiments the influence of electric current on phase coarsening is much greater than the possible influence of the thermomigration due to Joule heating during current stressing.

Since Pb phase growth of solder joint under current stressing is closely related to the current density as clearly shown in Fig. 7, we propose a phase growth evolution to include the influence of electric current by adding a current density term to Burke's grain growth equation

$$d^n - d_0^n = K j^m t,$$

where j is the current density, m is the exponent for current density. The normalized form is then

$$\frac{d}{d_0} = \left(1 + \frac{K}{d_0^n} j^m t\right)^{\frac{1}{n}}.$$

Let $Z = d/d_0$, $X = t$, $Y = j$, $B_1 = K/d_0^n$, $B_2 = n$, and $B_3 = m$. We are now using the experimental data of all the solder joints to fit a single equation $Z = (1 + B_1XY^{B_3})^{1/B_2}$, which involves two independent variables X (time) and Y (current density). The regression result is shown in Table 3. The exponent n is found to be about 5.5, and current density exponent m is about 3. The phase growth exponent n calculated in this model, 5.5, is close to the growth exponent calculated in Burke's grain growth model without current, 4.4–6.2. The comparison between the fitted surface and test data is shown in Fig. 10.

Table 3

Nonlinear regression results with two independent variables

Parameters	Value	Standard error	t -value	90.00% Confidence limits		$P > t $
B_1	0.14987989	0.030990236	4.836358518	0.098211774	0.201548005	0.00001
$B_2 = n$	5.510654291	0.440952065	12.49717312	4.77548201	6.245826572	0.00000
$B_3 = m$	3.065412008	0.244324285	12.54648921	2.658065141	3.472758875	0.00000

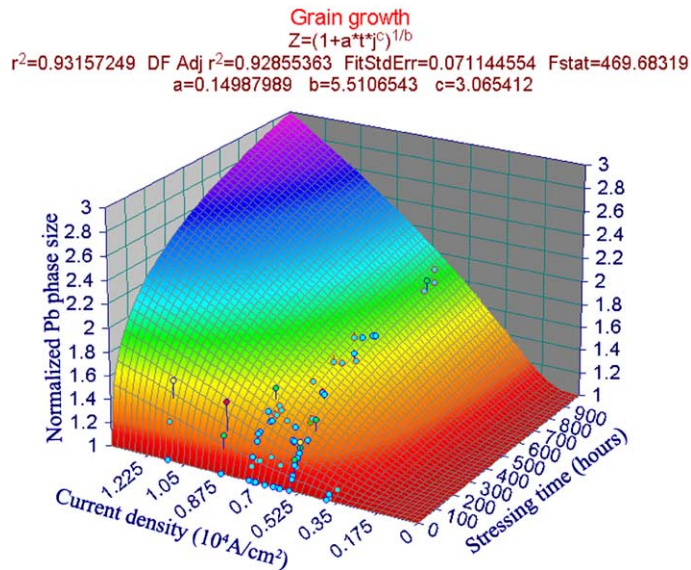


Fig. 10. Regression of grain growth including the influence of current density.

6. Conclusions

Experimental research on the Pb phase coarsening of eutectic Pb/Sn flip chip solder joint under current stressing is reported. Phase growth is observed under different current density and temperature. Higher current density leads to faster grain coarsening. Based on the test results, a grain coarsening equation including the influence of current density is proposed, $d^n - d_0^n = K j^m t$. The current density exponent m is found to be 3, and phase growth exponent n is found to be 5.5. Electric current seems to have a greater influence on phase growth in solder joints than temperature or thermomigration caused by the temperature gradient due to joule heating during current stressing in our test temperature range. The theoretical explanations for $n \approx 5.5$ and $m = 3$ are not clear.

Acknowledgements

This project is provided by the Office of Naval Research Advanced Electrical Power Systems under the supervision of Mr. Terry Ericson. Thanks Dr. Darrel Frear and Dr. Jong-Kai Lin from Motorola Inc. for providing us all of the flip chip test vehicles.

References

- Basaran, C., Chandaroy, R., 1998. Mechanics of Pb40/Sn60 near-eutectic solder alloys subjected to vibrations. *Applied Mathematical Modelling* 22 (8), 601–627.
- Basaran, C., Tang, H., 2001. Computer simulations of solder joint reliability tests. *Advanced Packaging Magazine*.
- Brandenburg, S., Yeh, S., 1998. Electromigration studies of flip chip bump solder joints. *Surface Mount International Conference Proceedings*.
- Burke, J.E., Turnbull, D., 1952. *Progress in Metal Physics*, vol. 3. Pergamon Press, London. p. 220.
- Chen, L.C., Spaepen, F., 1991. Analysis of calorimetric measurements of grain growth. *Journal of Applied Physics* 69 (2), 679–688.

- Chen, S.-W., Chen, C.-M., Liu, X., 1998. Electric current effects upon the Sn\Cu and Sn\Ni interfacial reactions. *Journal of Electronic Materials* 28 (11), 1193–1197.
- Chow, C.L., Wei, Y., 1999. Constitutive modeling of material damage for fatigue failure prediction. *International Journal of Damage Mechanics* 8 (4), 355–375.
- Conrad, H., 2000. Effects of electric current on solid state phase transformations in metals. *Materials Science and Engineering, A: Structural Materials: Properties, Microstructure and Processing* 287 (2), 227–237.
- Dasgupta, A., Hu, J.M., 1992. Failure mechanism models for ductile fracture. *IEEE Transactions on Reliability* 41 (4), 489–495.
- E1382 Standard Test Methods for Determining Average Grain Size Using Semiautomatic and Automatic Image Analysis, Annual book of ASTM standards, ASTM, 1999a.
- E3 Standard Methods of Preparation of Metallographic Specimens, Annual book of ASTM standard, ASTM, 1999b.
- Frear, D.R., Burchett, S.N., Neilsen, M.K., Stephens, J.J., 1997. Microstructurally based finite-element simulation of solder joint behavior. *Soldering & Surface Mount Technology* 25, 39–42.
- Hacke, P., Sprecher, A.F., Conrad, H., 1993. Computer simulation of thermomechanical fatigue of solder joints including microstructure coarsening. *Journal of Electronic Packaging* 115 (2), 153–158.
- Jung, K., Conrad, H., 2001a. Microstructure coarsening during static annealing of 60Sn40Pb solder joints: I stereology. *Journal of Electronic Materials* 30 (10), 1294–1302.
- Jung, K., Conrad, H., 2001b. Microstructure coarsening during static annealing of 60Sn40Pb solder joints: II eutectic coarsening kinetics. *Journal of Electronic Materials* 30 (10), 1303–1307.
- Kirchheim, R., 1992. Stress and electromigration in Al-lines of integrated-circuits. *Acta Metallurgica et Materialia* 40 (2), 309–323.
- Koppelaar, T.J., Simcoe, C.R., 1963. The effect of electric current on the aging of an Al-4%Cu alloy. *Transactions of the AIME* 227, 615–617.
- Lai, Z.H., Conrad, H., Chao, Y.S., Wang, S.Q., Sun, J., 1989. Effect of electropulsing on the microstructure and properties of iron-based amorphous-alloys. *Scripta Metallurgica* 23 (3), 305–310.
- Lai, Z.H., Chao, Y.S., Conrad, H., Chu, K., 1995. Hyperfine-structure changes in iron-base amorphous-alloys produced by high-current density electropulsing. *Journal of Materials Research* 10 (4), 900–906.
- Lee, T.Y., Tu, K.N., 2001. Electromigration of eutectic SnPb and SnAg3.8Cu0.7 flip chip solder bumps and under-bump metallization. *Journal of Applied Physics* 90 (9), 4502–4508.
- Lee, T.Y., Tu, K.N., Kuo, S.M., Frear, D.R., 2001. Electromigration of eutectic SnPb solder interconnects for flip chip technology. *Journal of Applied Physics* 89 (6), 3189–3194.
- Liu, W.-C., Chen, S.-W., Chen, C.-M., 1998. The Al/Ni interfacial reactions under the influence of electric current. *Journal of Electronic Materials* 28 (1), L5–L8.
- Liu, C.Y., Chen, C., Liao, C.N., Tu, K.N., 1999. Microstructure-electromigration correlation in a thin stripe of eutectic SnPb solder stressed between Cu electrodes. *Applied Physics Letters* 75 (1), 58–60.
- Liu, C.Y., Chen, C., Tu, K.N., 2000. Electromigration in Sn–Pb solder strips as a function of alloy composition. *Journal of Applied Physics* 88 (10), 5703–5709.
- Maurer, R., Gleiter, H., 1985. The effect of the electronic-structure on the behavior of grain-boundaries in metals. *Scripta Metallurgica* 19 (8), 1009–1012.
- Morris J.W., J.W., Tribula, D., Summers, T.S.E., 1991. The role of microstructure in thermal fatigue of Pb–Sn solder joints. In: Lau, John H. (Ed.), *Solder Joint Reliability*. Van Nostrand Reinhold, New York, pp. 225–265.
- Ng, H.P., Ngan, A.H.W., 2002. An in situ transmission electron microscope investigation into grain growth and ordering of sputter-deposited nanocrystalline Ni3Al thin films. *Journal of Materials Research* 17 (8), 2085–2094.
- Solomon, H.D., 1986. Creep, strain rate sensitivity, and low-cycle fatigue of 60/40 solder. *Brazing & Soldering* 11, 68–75.
- Solomon, H.D., Tolsdorf, E.D., 1996. Energy approach to the fatigue of 60/40 solder. 2. Influence of Hold time and asymmetric loading. *Journal of Electronic Packaging* 118 (2), 67–71.
- Teng, G.Q., Chao, Y.S., Lai, Z.H., Dong, L., 1996. Microstructural study of the low-temperature nanocrystallization of amorphous Fe78B13Si9. *Physica Status Solidi A—Applied Research* 156 (2), 265–276.
- Tu, K.N., Zeng, K., 2001. Tin–lead (Sn–Pb) solder reaction in flip chip technology. *Materials Science & Engineering, R: Reports* 34 (1), 1–58.
- Upadhyayula, K.S., 1999. An incremental damage superposition approach for surface mount electronic interconnect durability under combined temperature and vibration environments. PhD dissertation, University of Maryland.
- User Manual: Image Pro Plus, ver. 3.01, Media Cybernetics Inc., 2000.
- Xu, Z.S., Lai, Z.H., Chen, Y.X., 1988. Effect of electric-current on the recrystallization behavior of cold-worked Alfa-Ti. *Scripta Metallurgica* 22 (2), 187–190.
- Ye, H., Basaran, C., Hopkins, D., 2002a. Experiment study on reliability of solder joints under electrical stressing–nano-indentation, atomic flux measurement. In: *Proceedings of 2002 International Conference on Advanced Packaging and Systems*, Reno, Nevada, March 2002.

- Ye, H., Basaran, C., Hopkins, D.C., 2002b. Mechanical implications of high current densities in flip chip solder joints. In: Proceedings of ASEM International Mechanical Engineering Congress and Exposition, Orleans, LA, November 2002.
- Ye, H., Basaran, C., Hopkins, D., 2003a. Mechanical degradation of microelectronics solder joints under current stressing. *International Journal of Solids and Structures* 40 (26), 7269–7284.
- Ye, H., Basaran, C., Hopkins, D., 2003b. Thermomigration in Pb–Sn solder joints under Joule heating during electric current stressing. *Applied Physics Letters* 82 (8), 1045–1047.
- Ye, H., Hopkins, D.C., Basaran, C., 2003c. Measurement of high electrical current density effects in solder joints. *Microelectronics Reliability* 43 (12), 2021–2029.